



FIG. 1 To enable successful timing convergence, the synthesis tool must identify the critical path and accurately predict its delay. To achieve maximum frequency and reasonable timing closure, Agilent strives to keep synthesis timing error below 10 percent of the design's clock period.

delay. At 0.25 micron, wire delays due to propagation delay in the wire itself also become significant. And at 0.18 micron, delays arising from wires often exceed gate delays on critical paths.

The WLM has been the traditional statistical method of coupling synthesis timing with post-artwork timing. For smaller process technologies, interconnect exerts a greater influence on overall delay and WLM-based timing correlates less with post-artwork timing.

Synthesis tool writers have looked into the wire parasitic problem and realized that it is quite complicated. A wire can be described by several factors, including length, width, neighboring wires, gate loading and fan-out. Gate loading and fan-out are the “knobs” that are directly controlled by synthesis. WLMs make the assumption that fan-out can predict a wire's parasitics. Therefore, in a single integer—that is, fan-out—synthesis tools have tried to wrap up an extremely complicated problem.

Differentiating physical synthesis tools, like Synopsys' Physical Compiler, is being able to use their knowledge of placement to make more accurate estimates of wire delay. Unlike WLMs, which are based on statistical distribution of wires with a common fan-out, Physical Compiler estimates wire resistance and capacitance wire by wire.

For the physical synthesis tool to work quickly, it uses Steiner or half-perimeter estimates to calculate wire length for each net based on the locations of the pins to which it is attached. Currently, Physical Compiler uses a

lumped RC model based on horizontal and vertical resistance and capacitance parameters for the wires. These location-based estimates provide a much more accurate prediction of post-route timing.

The impact of block size

The longest possible wire in a block, barring a meandering route, runs from corner to corner, horizontally across the width of the block and vertically across its height. Thus, a block's half-perimeter bounds the worst-case, direct, point-to-point route. Similarly, it bounds direct multiple fan-out nets.

As blocks grow, so do their half-perimeters. So for any process larger blocks tend to have longer wires. Although some wires in a large block are short, there are generally several that are quite long that result in large wire capacitance and resistance and long wire delays. Consequently, larger blocks are increasingly susceptible to larger wire delays.

Furthermore, not all routes are direct. As they meander to avoid localized congested hot spots, WLM and even physical synthesis estimates become less accurate. Just as growing block size increases variance from WLM estimates, larger blocks are more susceptible to meander-induced error. Although physical synthesis greatly enhances the accuracy of timing prediction, it is still sensitive to increasing block size.

Fig. 1 shows how timing variance relates to block size in a 0.18-micron process. Each curve shows typical error for a synthesis prediction vs. actual extracted timing.