

# Software may help RF ICs keep pace with Moore's Law

Moore's Law sets a tough standard, but handset component suppliers are determined not to fall behind.

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When considering the RF-specific technology evolutions discussed recently, a common question emerges: Can RF technologies keep up with the scaling pace of Moore's Law?

From a physics perspective, the problems keep getting more difficult and we've already seen new architectures and a lot of investment to solve these issues. For various economic reasons, only focused large companies or the most innovative small companies are likely to be solution suppliers, and thus survivors in the market.

If Moore's Law doesn't apply, then the questions become what alternatives will be adopted for those cases in which an RF technology doesn't scale? How will a handset's RF section continue to get cheaper, or will filters or power amplifiers (PAs) ultimately set the price?

One trend anticipated in the implementation of next-generation wireless IC for mobile handsets is the need to coordinate research, development, and productization of new system architectures. This includes RF circuit designs, IC technologies, filter technologies, antennas, guided wave structures, electro-optic components, and, believe it or not, software. There's no doubt that CMOS has been selected as the technology of the future for wireless transceivers, leaving the PA and LNA functionality to SiGe and GaAs technology (but for how long?).

One central question is whether the expected rate of progress (we went from 0.25-micron RF CMOS in 2000 to 90-nm standard CMOS in 2006) will meet system electrical and cost requirements in the coming years. A major concern in CMOS scaling is sufficient process maturity and reliability so as to not impede the basic rate of CMOS scaling.

Because the performance of many RF components is tied to the performance of active devices, a significant effort in the last few years has been given to

productivity improvement by designing software-controllable active devices. This is particularly true for cellular handset RF ICs and even for non-silicon based devices, such as the PA and LNA.

Due to the higher data rate supported by next generation wireless systems and higher power consumption constraints, a large number of devices use an extensive amount of digital software processing to pre-condition the signal over the air in the transmit and receive paths. PA efficiencies, and thus handset talk-time, have been significantly increased using such techniques. The direct effect is including the PA circuit constraints in the transceiver design and dedicating significant processing power in the digital world to support such improvements.

Similarly on the receive side, while CMOS devices are capable of very low noise figures, the LNA is usually limited by electromagnetic interference coupled from logic or other on-chip analog circuitry. As a result, many of today's "transceivers on a chip" integrate all the active RF functions except the PA and LNA. In the future, the use of digital signal processing in the receive path will compensate for this. This approach doesn't necessarily resolve the interference problem coupled from logic, but with careful frequency planning this approach could help with the number of radio bands and integration expected to be integrated into handsets.

The physical size of RF bandpass filters and multiplexers are generally inversely proportional to the center frequency. This implies a new filter technology for size reduction. Although some of the most promising of these technologies are film bulk acoustic resonator (FBAR) filters, new filter architectures employ software-enhanced tuning filters and passband to provide better test costs, new test approaches, and configurability for different protocols.

In the past, a significant difference between PCs and handsets is that PCs

continuously compete on performance (CPU clock speed and computational throughput). In contrast, handsets specify most of the receiver and transmitter functionality (bandwidth, transmit power, or receiver noise figure) and handset functions (talk time, number of bands). In the future, we could expect to see an increased interest by designers in CPU performance for RF functionality to cope with multiple protocol RF support.

The addition of software in the transceiver not only improves performance and functionalities and changes the architecture, it also impacts design methodology and will significantly change how RF IC designers approach their designs and architectures. We're already seeing 8-bit microprocessors in the transceiver path and synthesizers to increase clock accuracy, compensate for quantization and noise errors, tuning, and configurability issues of multi-band and multi-protocol support. It's only a question of time before we see larger processors relying and more complex software.

Note that I'm not implying that software is the solution for RF ICs to meet Moore's Law. But if you include this trend with the other design and process innovations seen last year, there are reasons to be optimistic. It won't be easy to keep pace with Moore's Law, but RF IC designers keep exceeding expectations. While 90 nm was perceived as a significant barrier just 5 years ago, 65-nm CMOS is now upon us.

## About the author

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